REMARKS

Pending Claims

Claims 1, 3, 6 and 8 have been amended. Claims 2, 4 and 7 have been canceled. No new claims have been added. Accordingly, claims 1, 3, 5, 6 and 8 remain pending in this application.

Claim Rejections under 35 U.S.C. §103

Claims 1 and 6-8 stand rejected under 35 U.S.C. §103(a) as being unpatentable over Katz, U.S. Patent No. 3,521,242 (hereafter "Katz") in view of Yamada, U.S. Patent No. 5,986,924 (hereafter "Yamada"). Claims 2-5 stand rejected under 35 U.S.C. §103(a) as being unpatentable over Katz and Yamada, as applied to claim 1, and further in view of Kotani, U.S. Patent No. 6,638,799 (hereafter "Kotani"). Applicants respectfully traverse the rejections, and request reconsideration and withdrawal of the rejections for the following reasons.

The present invention provides a semiconductor device mounted with a SRAM memory using a SOI substrate that ensures stable operation while meeting limited space requirements. In the memory cell formed on the SOI substrate, the regions forming channels of the transfer N-channel type MISFETs are coupled at their gates. This structure of Applicants' invention is able to be manufactured by removing a portion of a gate insulating film to conduct the channel formation regions of the

N-channel type MISFETs to the fixed power wiring line (see, e.g., Applicants' specification at page 12, line 16, through page 14, line 8).

Katz is cited for teaching certain aspects of Applicants' invention, but Katz fails to teach a memory cell formed on a SOI substrate in which the regions forming channels of the transfer N-channel type MISFETs are coupled at their gates. Yamada, at FIG. 2, is cited as teaching coupling of transistors 21, 22 to a first wiring line WL0 and the respective gates. However, Yamada teaches a bulk silicon substrate in the embodiments of FIGS. 1-6, rather than a SOI substrate (see, e.g., Yamada at col. 6, lines 51-59, FIG. 6, substrate 40, etc.). Further, while Yamada adopts a SOI base substrate in the embodiment of FIGS. 7-8, the gate 50 of the access transistor 22 is connected to the back gate 44, and not to the region forming the channel (see FIG. 8 and col. 7, lines 39-43). Thus, Yamada fails to teach Applicants' invention in which the regions forming channels of the transfer N-channel type MISFETs are coupled at their gates on a SOI substrate. Accordingly, the combination of Yamada with Katz, fails to teach or suggest Applicants' invention, as set forth in independent claims 1 and 6.

Kotani is relied upon for disclosing a memory device being on a chip with first and second semiconductor layers separated by an insulating layer. Thus, Kotani fails to make up for the deficiencies in the Katz and Yamada combination, as discussed above. Accordingly, independent claims 1 and 6 are allowable, and dependent claims 3, 5 and 8 are allowable at least because they depend from allowable base claims.

Conclusion

In view of the foregoing, Applicants respectfully request that a timely Notice of Allowance be issued in this case.

Respectfully submitted,

Colin D. Barnitz
Registration No. 35,061

MATTINGLY, STANGER, MALUR & BRUNDIDGE, P.C.
1800 Diagonal Rd., Suite 370
Alexandria, Virginia 22314
(703) 684-1120
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